



A DESIGN APPARATUS AND A METHOD FOR GENERATING AN
IMPLEMENTABLE DESCRIPTION OF A DIGITAL SYSTEM

Schaumont et al.

Appl. No.: 09/873,553 Atty Docket: IMEC65.1CP1C1

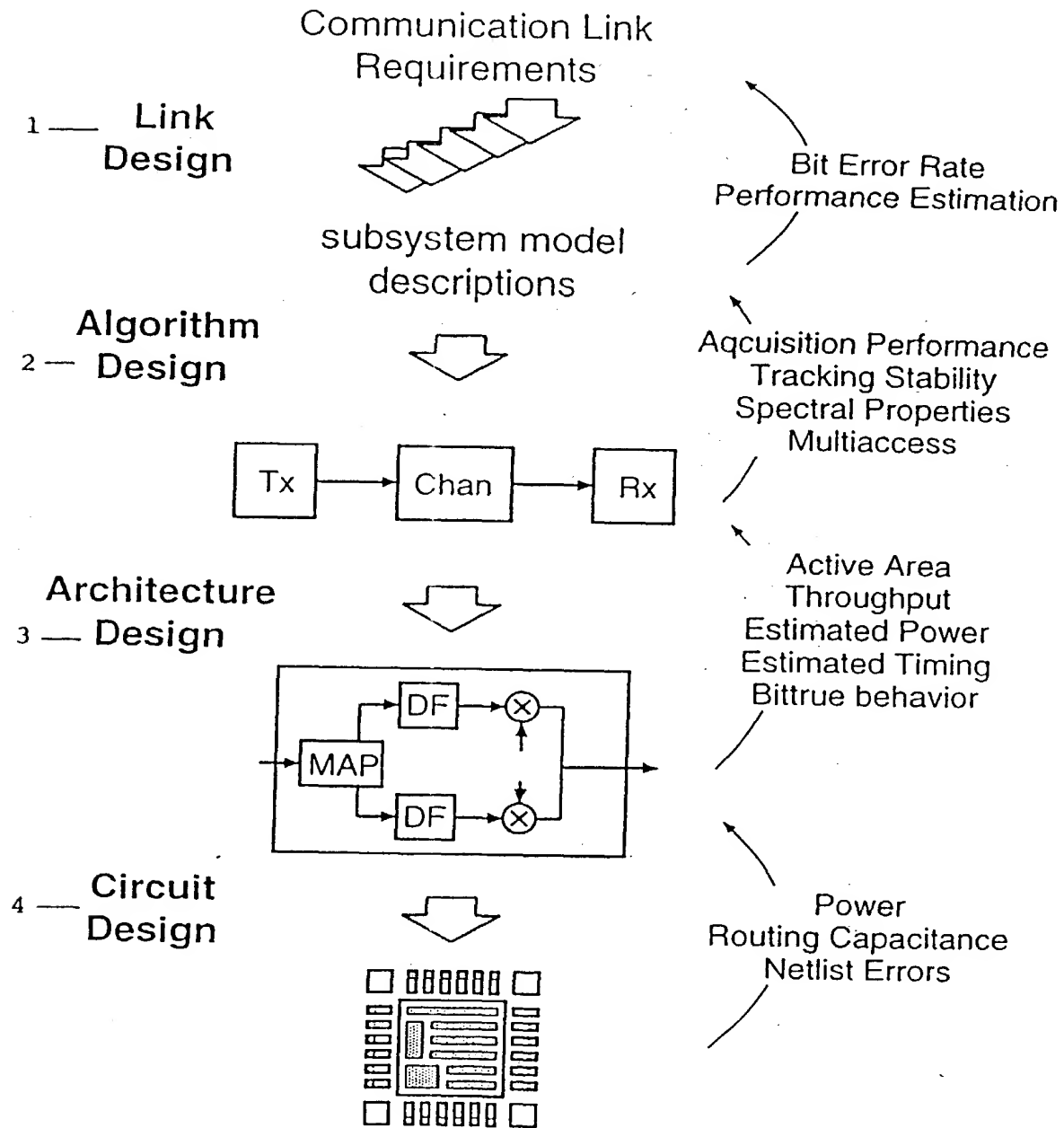


FIG. 1A

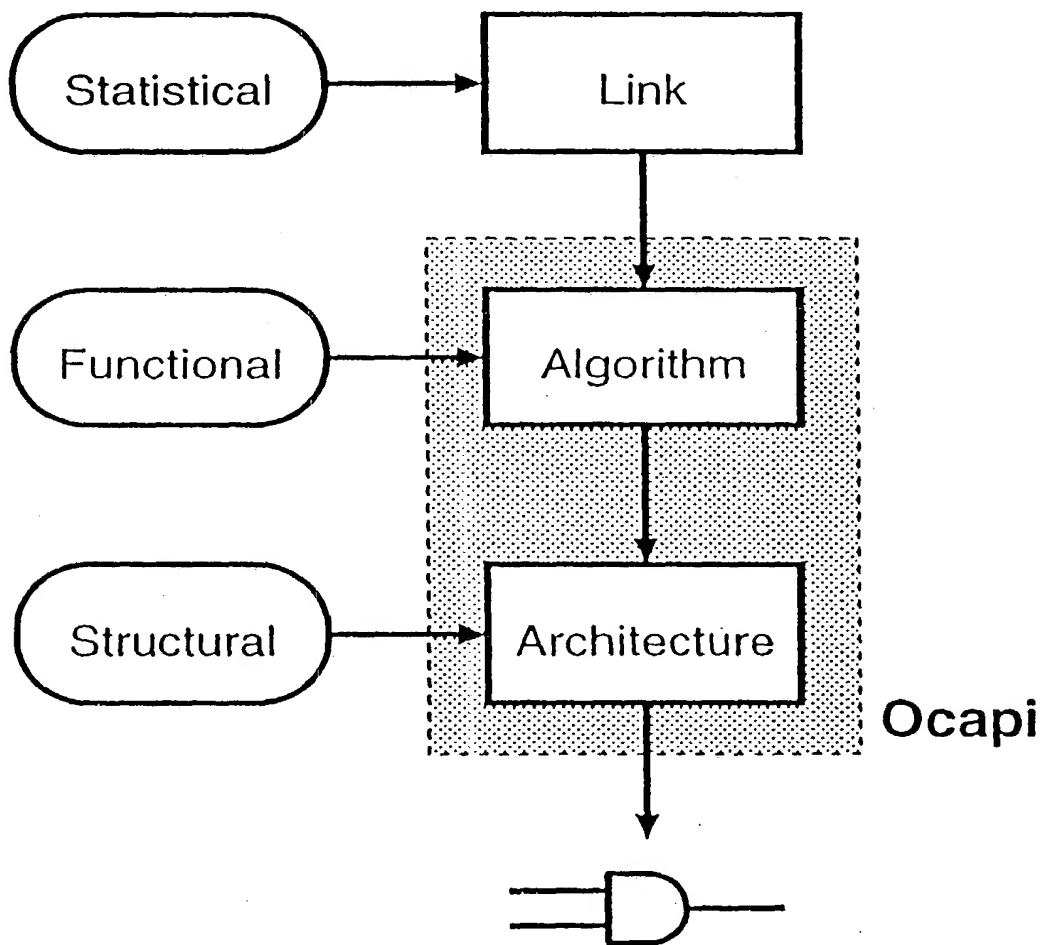


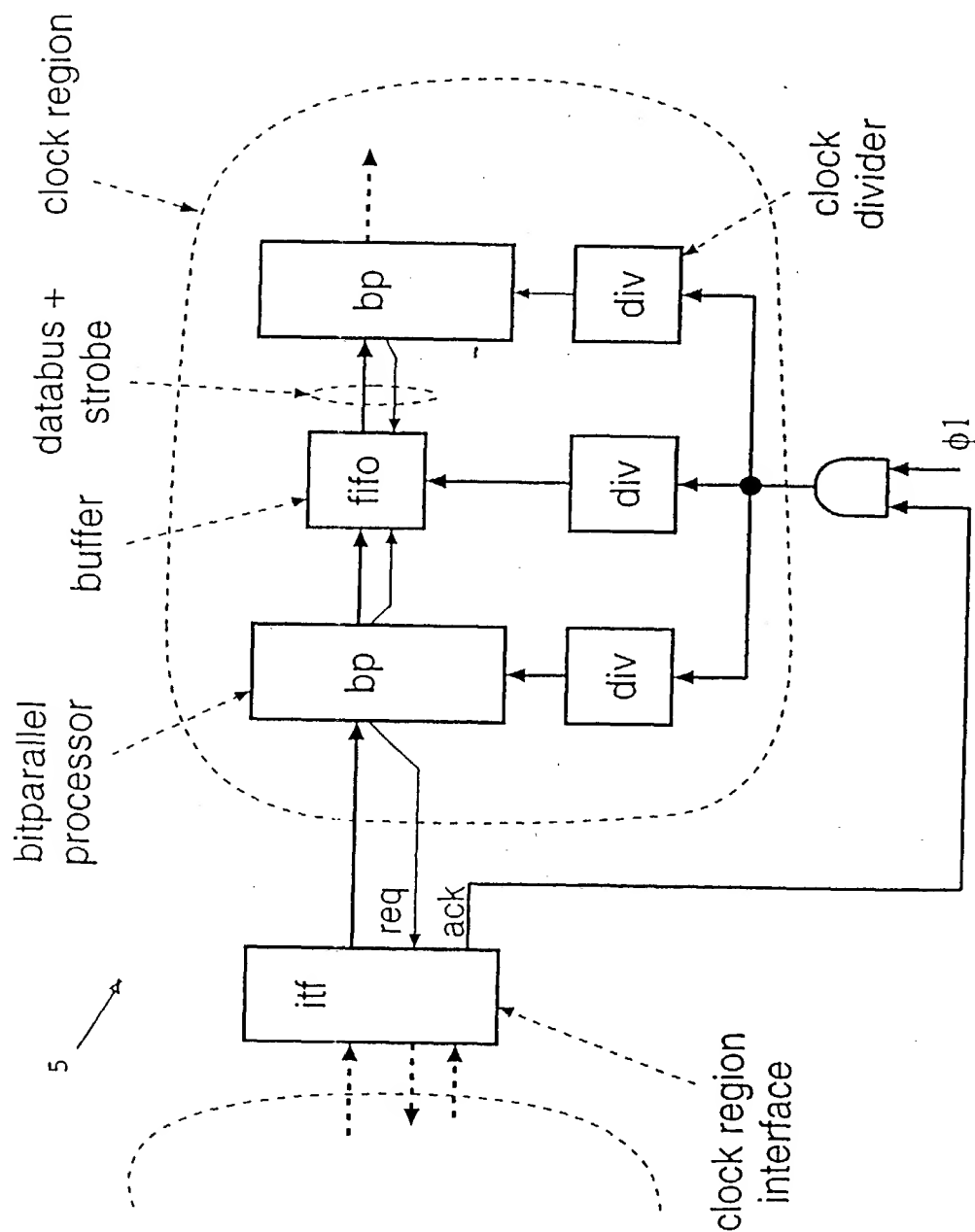
FIG. 1B



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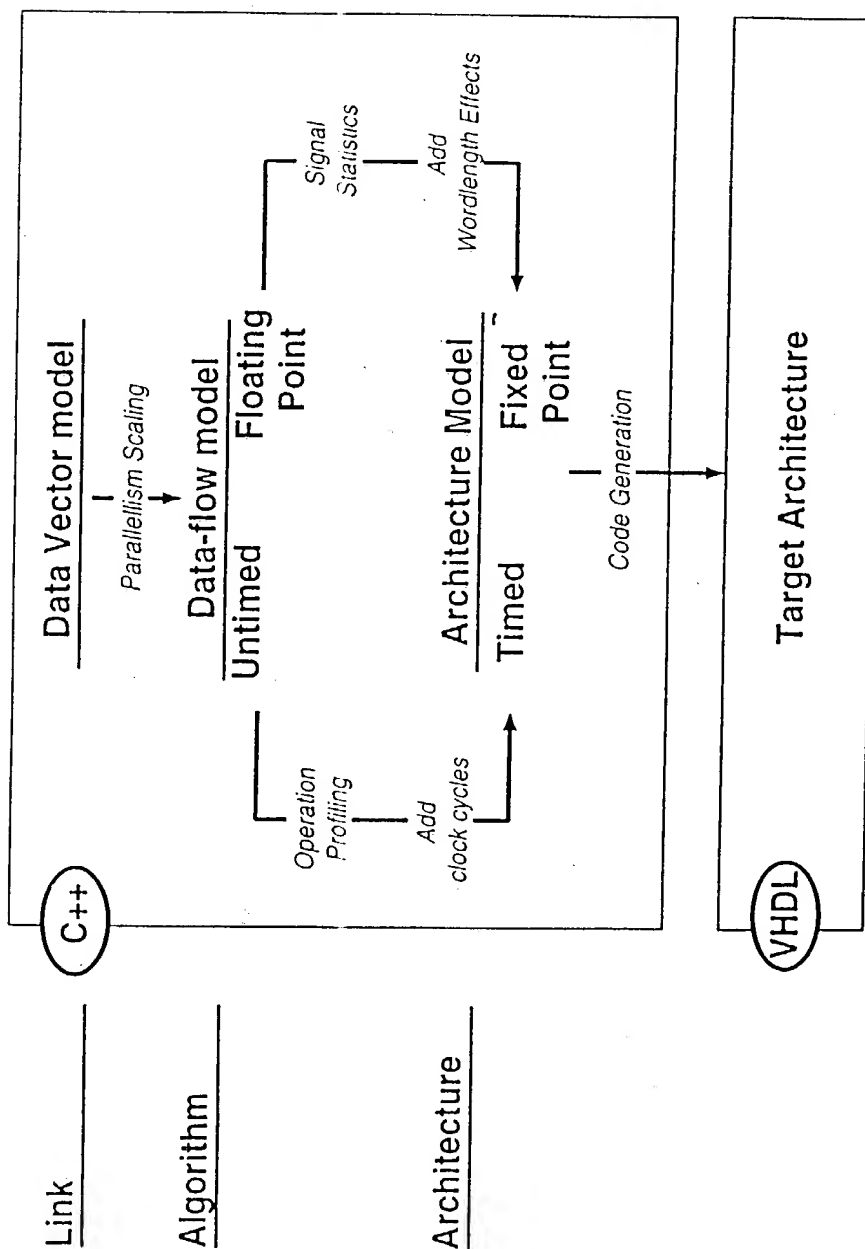


FIG. 3



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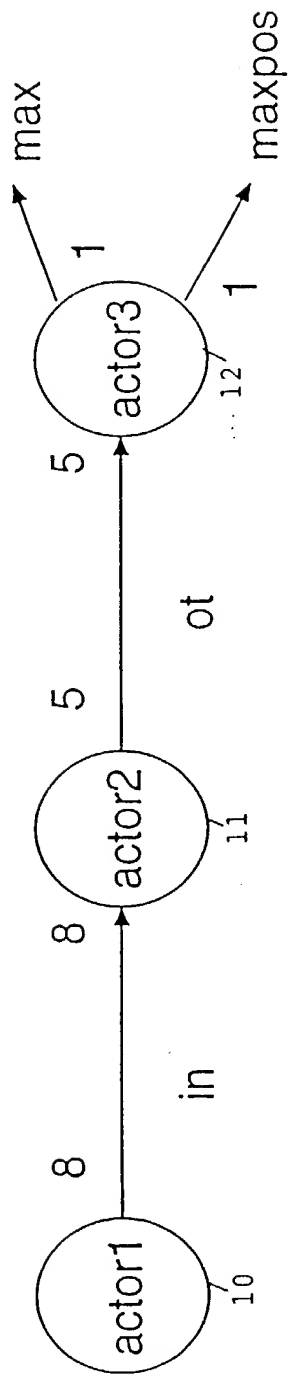


FIG. 4

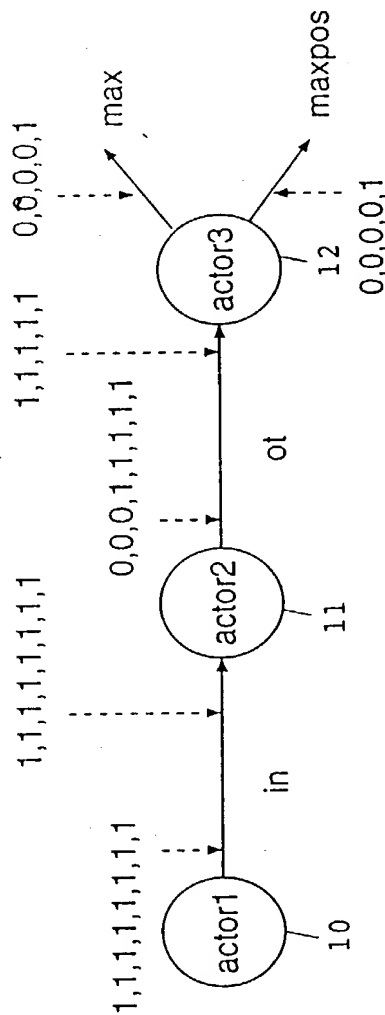


FIG. 5



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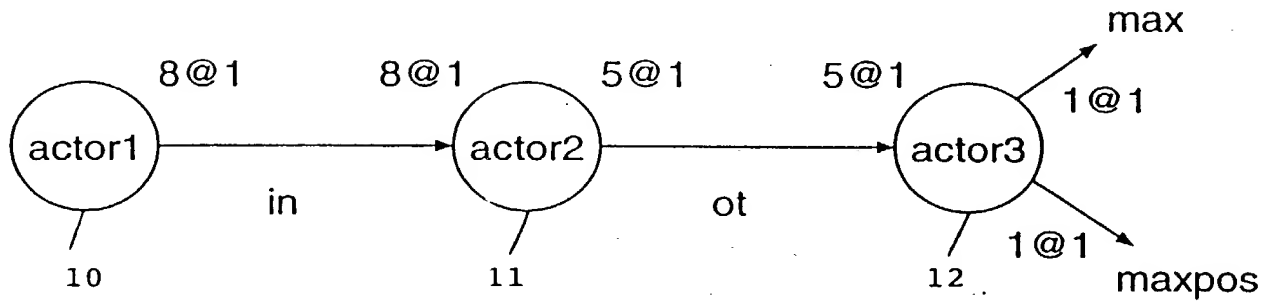


FIG. 6



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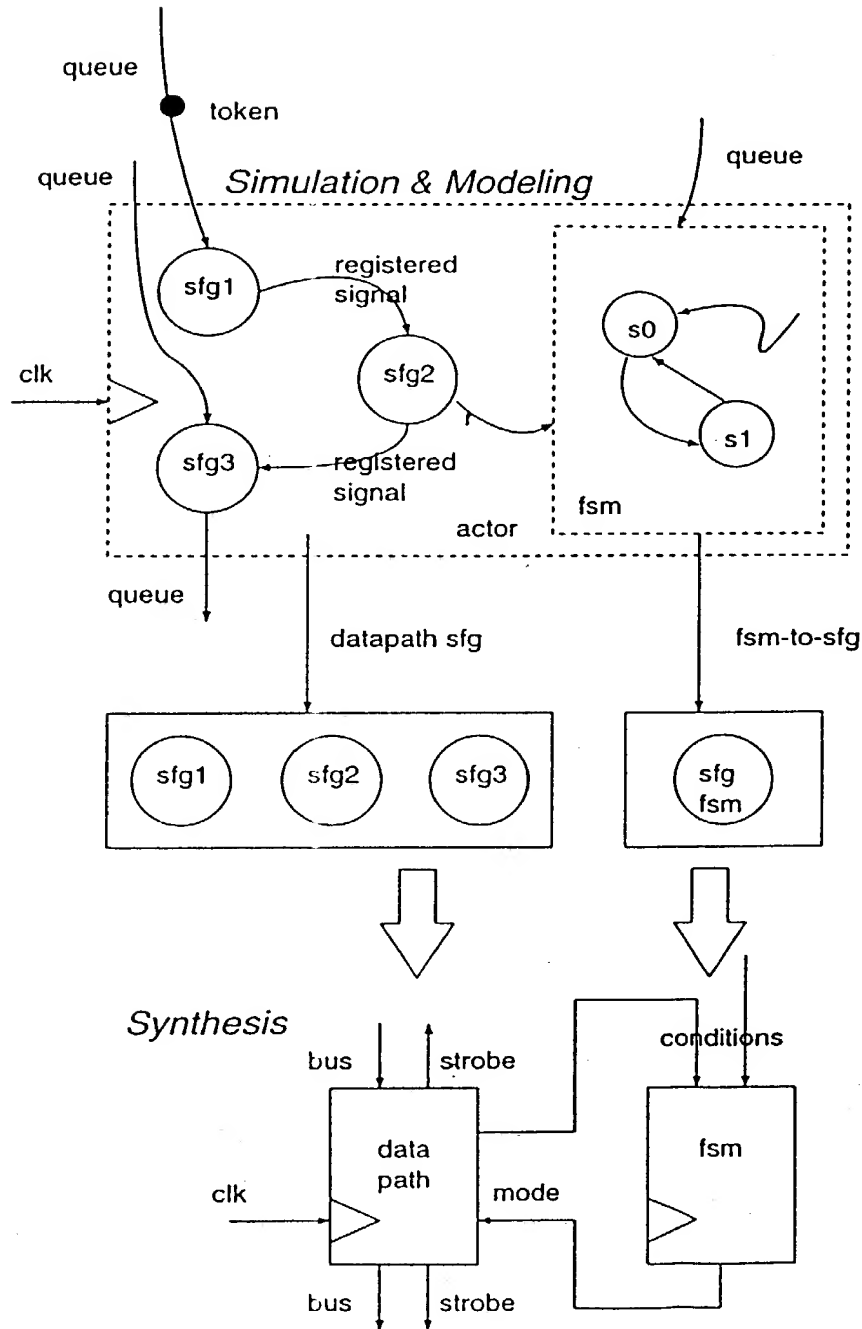


FIG. 7



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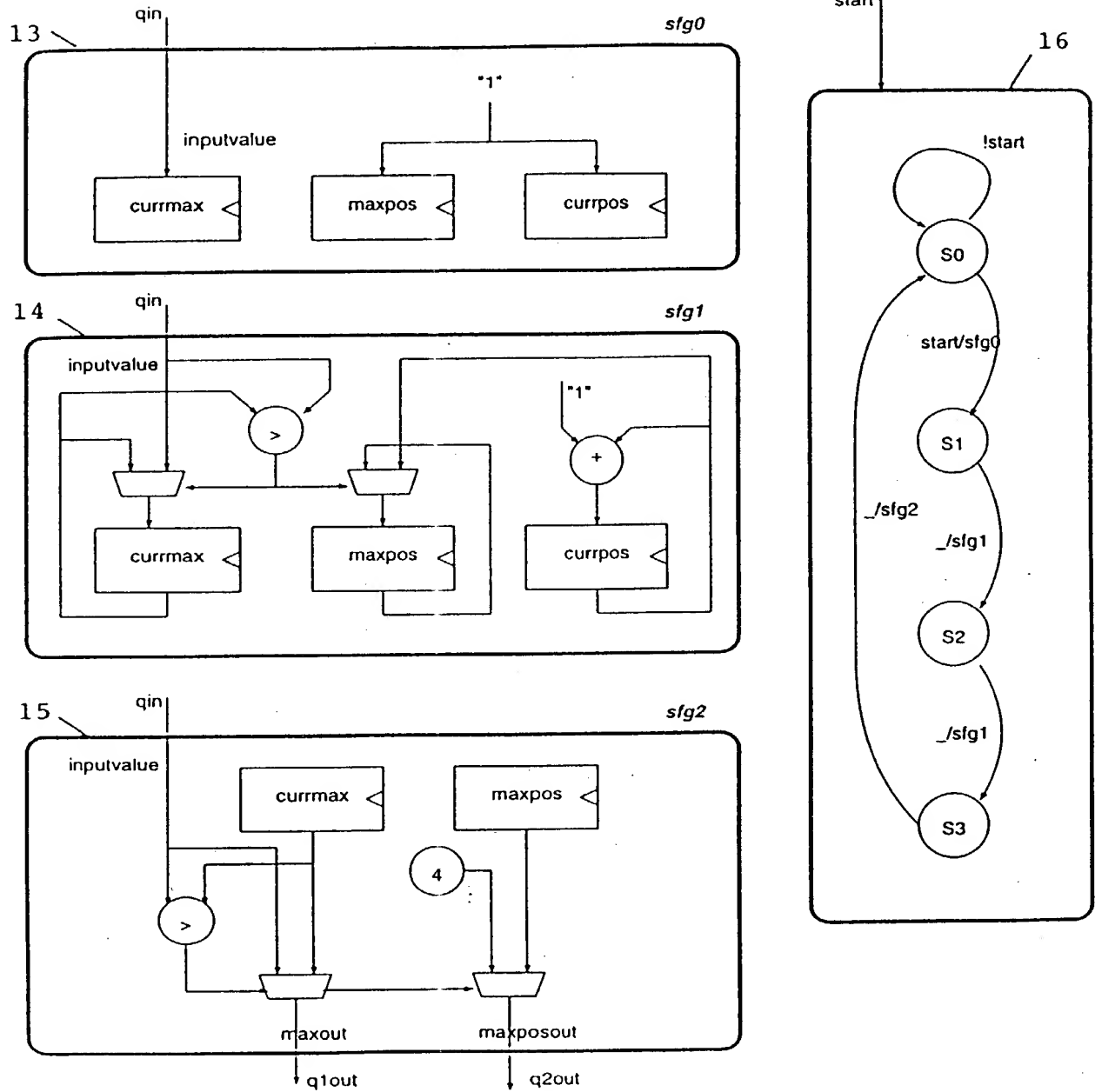


FIG. 8

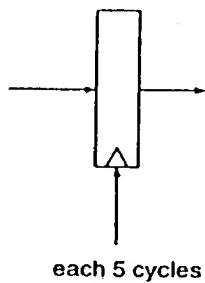


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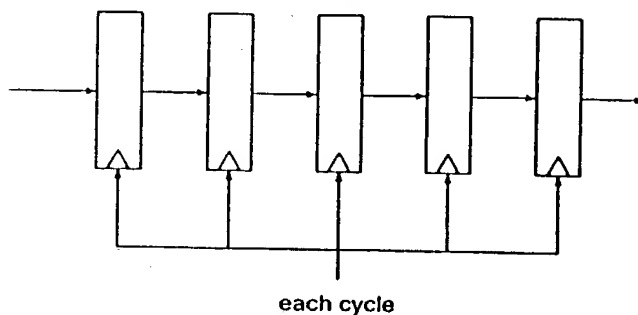
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travel delay = 5
token concurrency = 1
token latency = 5



travel delay = 5
token concurrency = 1
token latency = 1



travel delay = 5
token concurrency = 2
token latency = 1

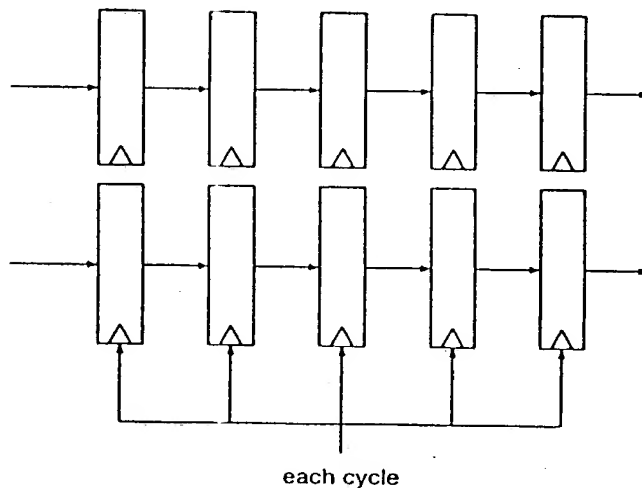


FIG. 9



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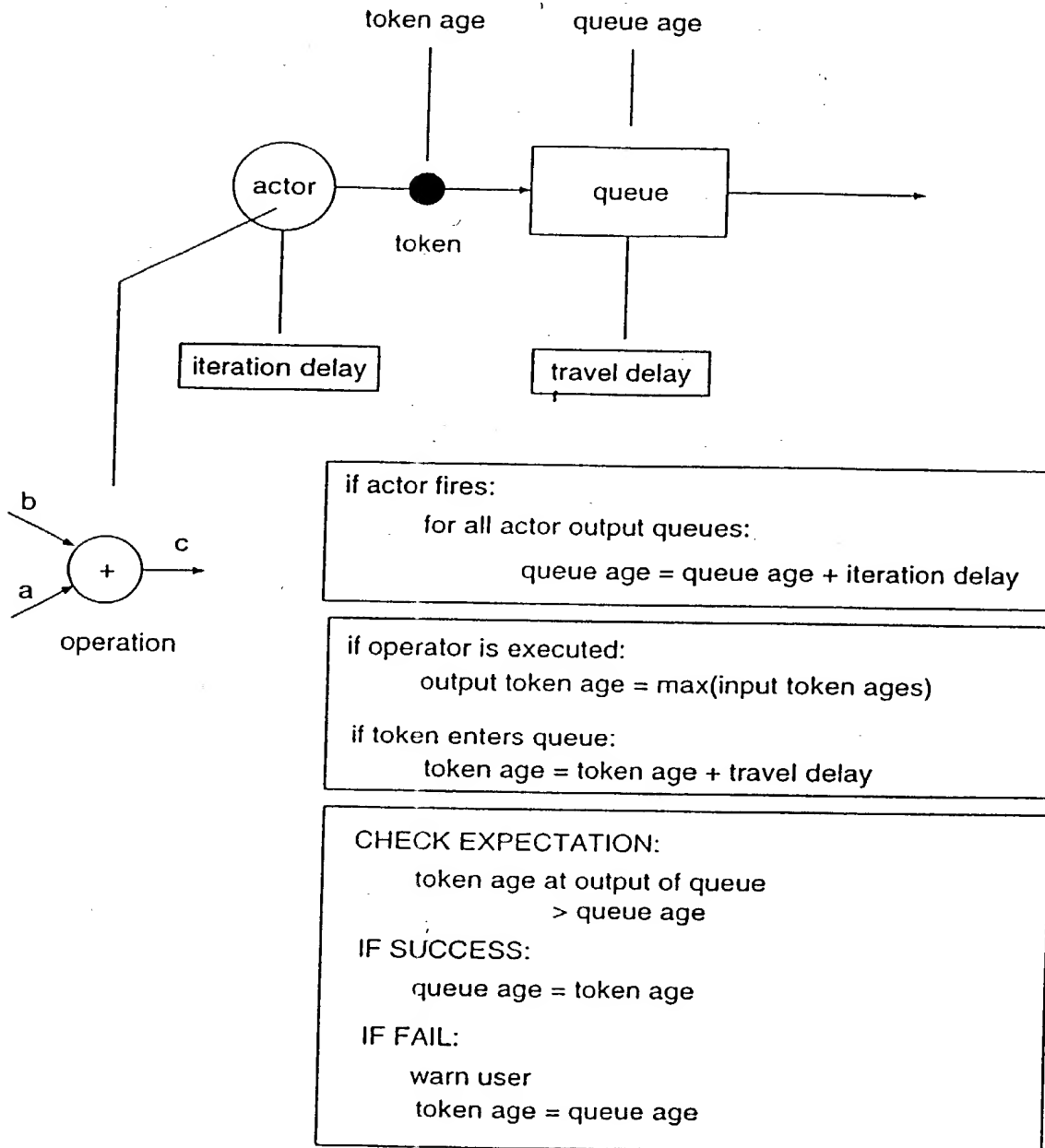


FIG. 10



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```
dfix T_sample(8, 6);
dfix T_acc (8, 6);
dfix T_bit (1, 0, ns);
double hardwired_coef = { 0.5, 0.2, -0.3, 0.15 };

fsm correlator::define(clk & _ck)
{
    sig_array coef (4, ck, T_sample);
    sig_array sample (4, ck, T_sample);
    sig accu (ck, T_accu );
    sig sample_in (T_sample );
    sig coef_in (T_sample );
    sig corr_out (T_sample );
    sig load (ck, T_bit );
    sig load_ctr (T_bit );

    sfg initialize_coefs;
    for (i = 0; i < 4; i++)
        coef[i] = W(T_sample, hardwired_coef[i] );

    sfg load_coef_0;
    input(coef_in);
    coef[0] = in_coef_in;

    sfg correl_1;
    accu = cast(T_acc, coef[0] * sample[0] + coef[1] * sample[1]);

    sfg correl_2;
    corr = accu + cast(T_acc, coef[2] * sample[2] + coef[3] * sample[3] );
    output(corr);

    sfg read_sample;
    input(sample_in);
    for (i = 3; i >= 0; i--)
        if (i)
            sample[i] = sample[i-1];
        else
            sample[i] = sample_in;

    sfg read_control;
    input(load_ctr);
    load = load_ctr;

    fsm myfsm;
    initial rst;
    state phase_1;
    state phase_2;
    rst << always << initialize_coefs << phase1;
    phase1 << always << read_control << phase2;
    phase2 << !cnd(load) << correl_1 << phase2;
    phase2 << cnd(load) << correl_2 << phase1;
    phase2 << cnd(load) << read_sample << phase1;
    phase2 << cnd(load) << read_sample << phase1;
    phase2 << cnd(load) << load_coef_0 << phase1;

    return myfsm;
}
```

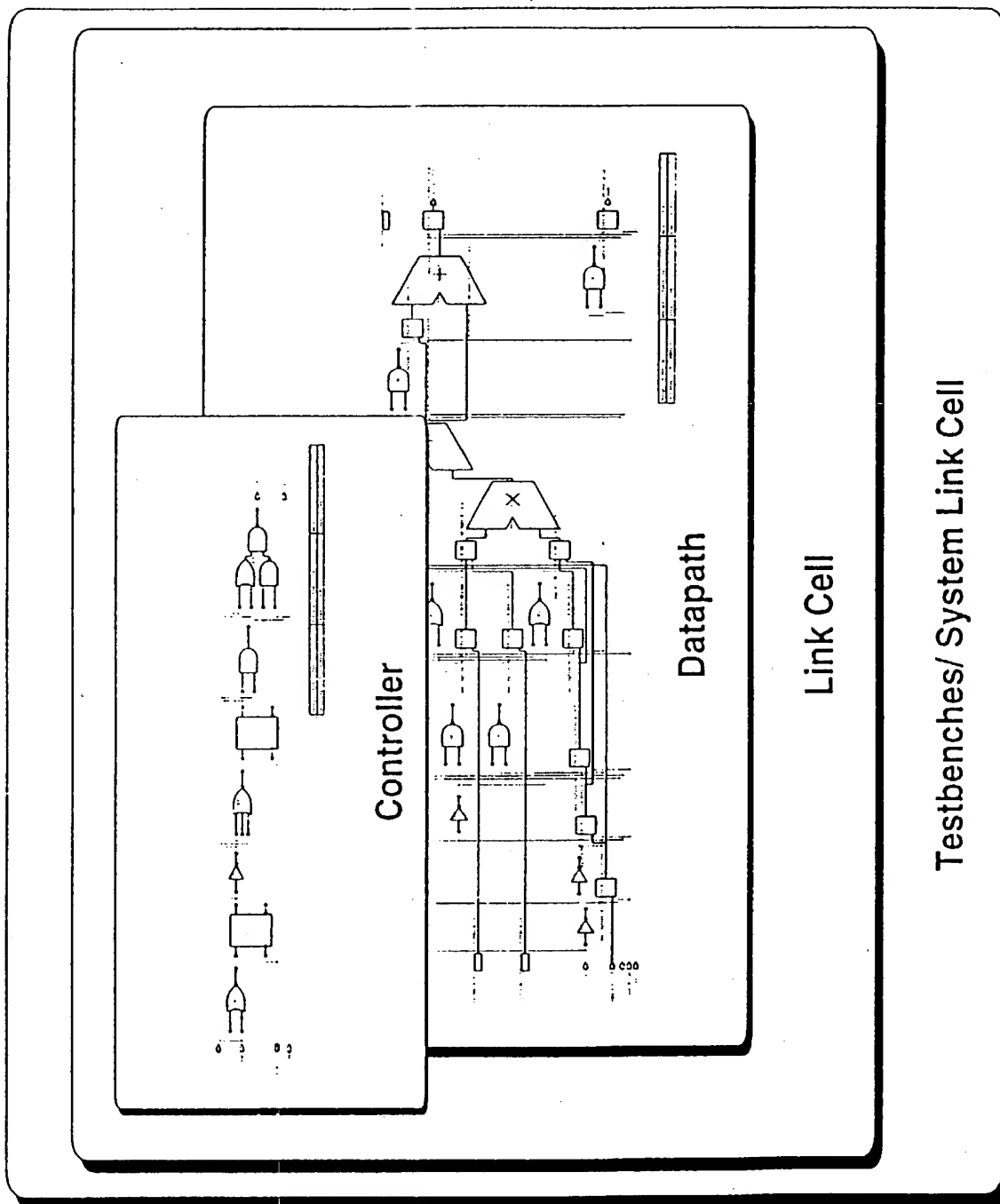
FIG. 11



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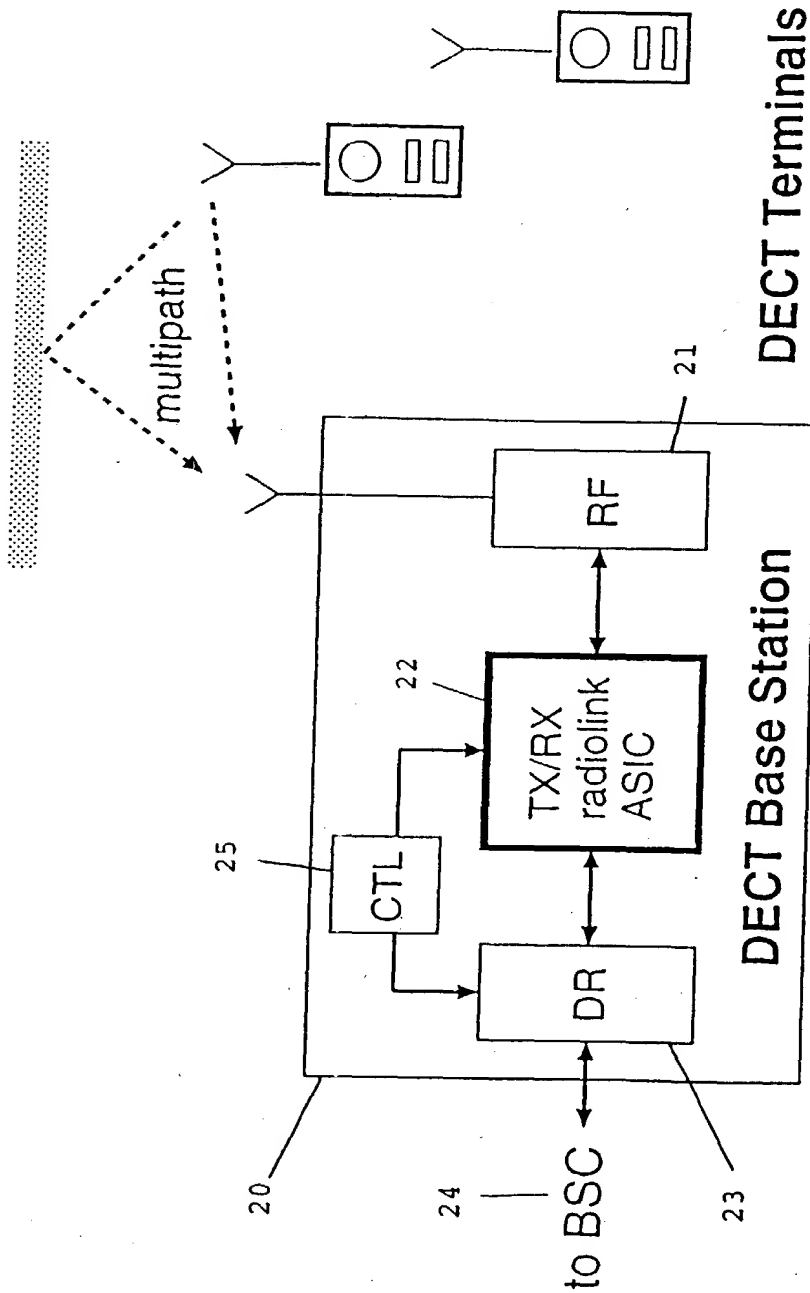


FIG. 13



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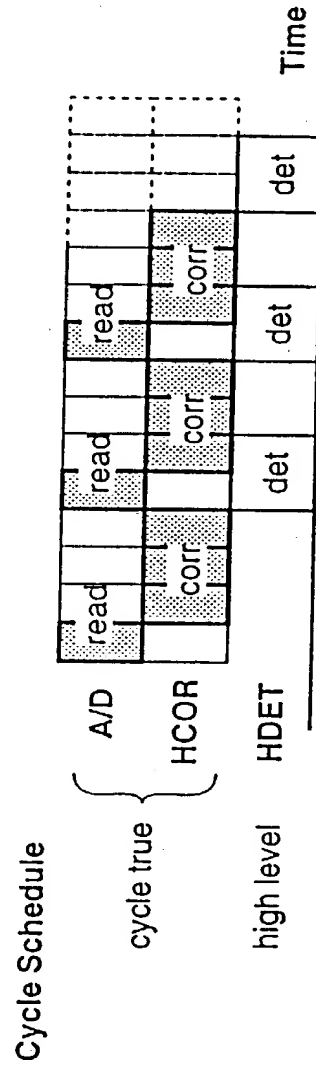
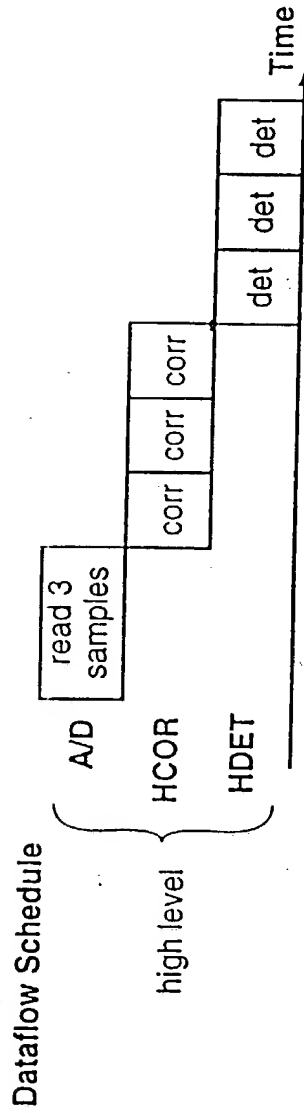
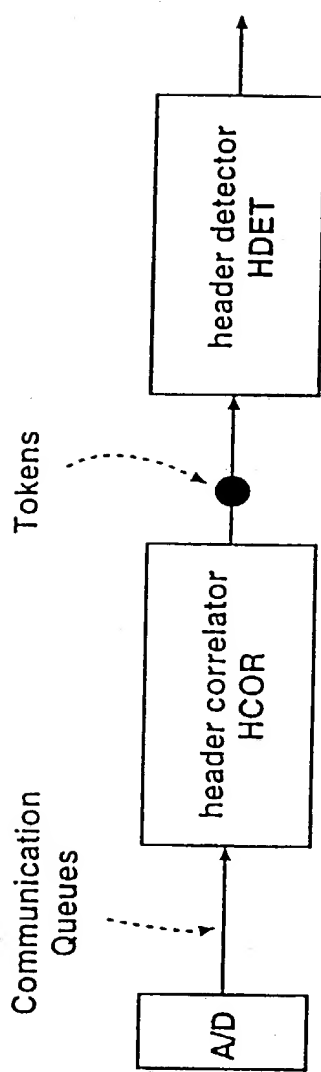


FIG. 14



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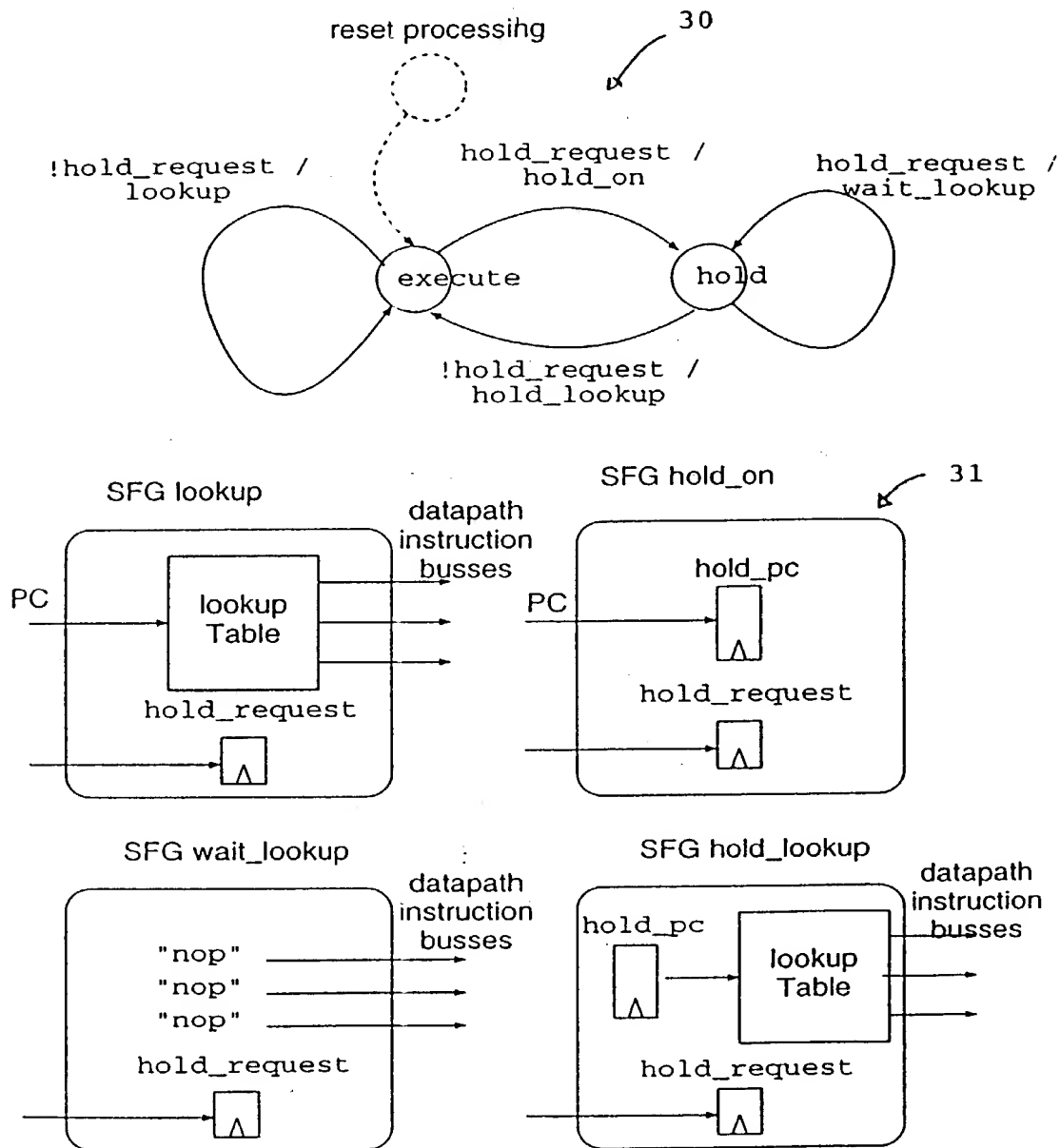


FIG. 15



15.

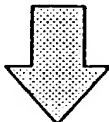
Sig Class

```
class sig {
    Value value;
    char *name;
public:
    sig(Value v);
    sig operator +(sig v);
    virtual Value simulate();
    virtual void gen_code(ostream &os);
};

sig sig::operator +(sig v) {
    sigadd s;
    add.left = &v;
    add.right = this;
    return add;
}

Value sig::simulate() {
    return value;
}

sig::gen_code(ostream &os) {
    os << name;
}
```



Derived Operator Class

```
class sigadd : public sig {
    sig *left;
    sig *right;
public:
    Value simulate();
    void gen_code(ostream &os);
};

Value sigadd::simulate() {
    return left->eval() +
           right->eval();
}

sigadd::gen_code(ostream &os) {
    os << left->cg()
       << " + "
       << right->cg();
}
```

FIG. 16



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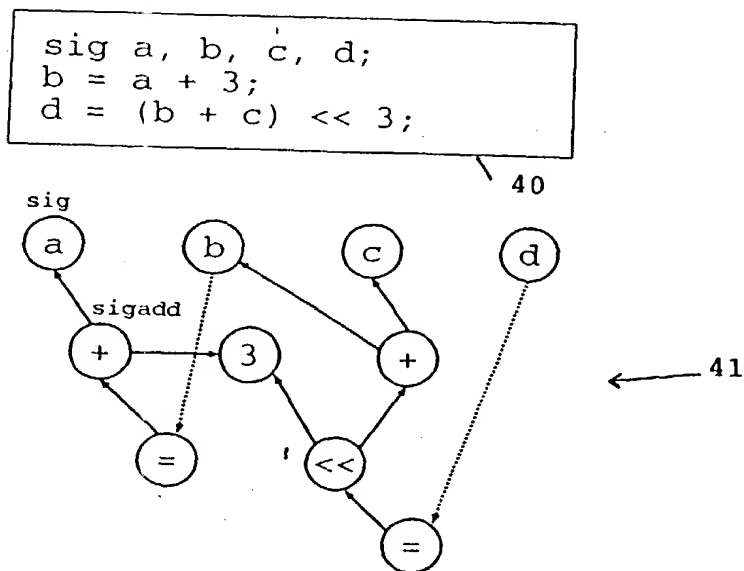
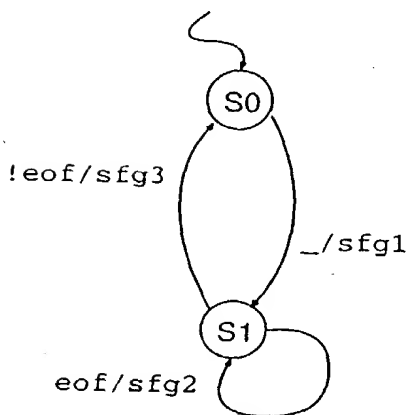


FIG. 17



```

fsm f;
initial s0;
state s1;

s0 << allways    << sfg1 << s1;
s1 << cnd.eof)  << sfg2 << s1;
s1 << !cnd.eof) << sfg3 << s0;
    
```

FIG. 18



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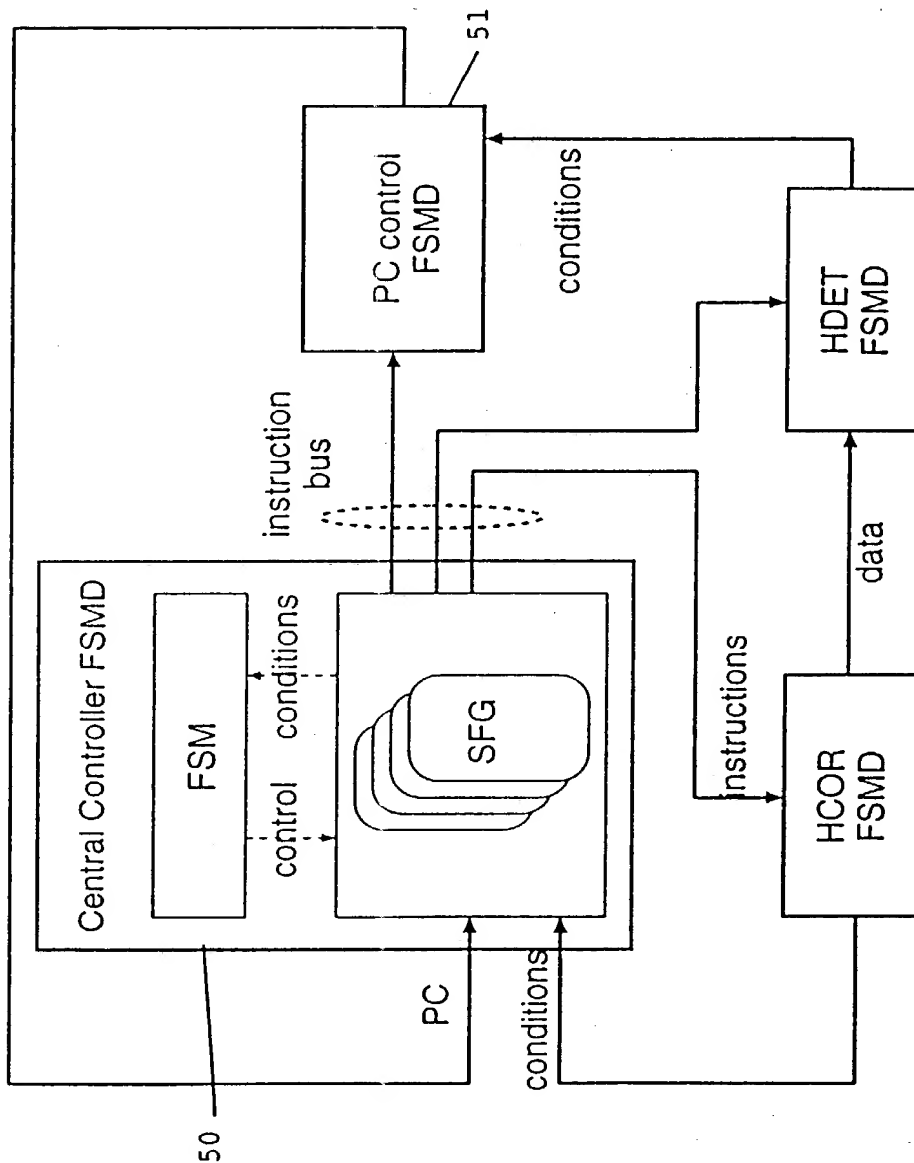


FIG. 19



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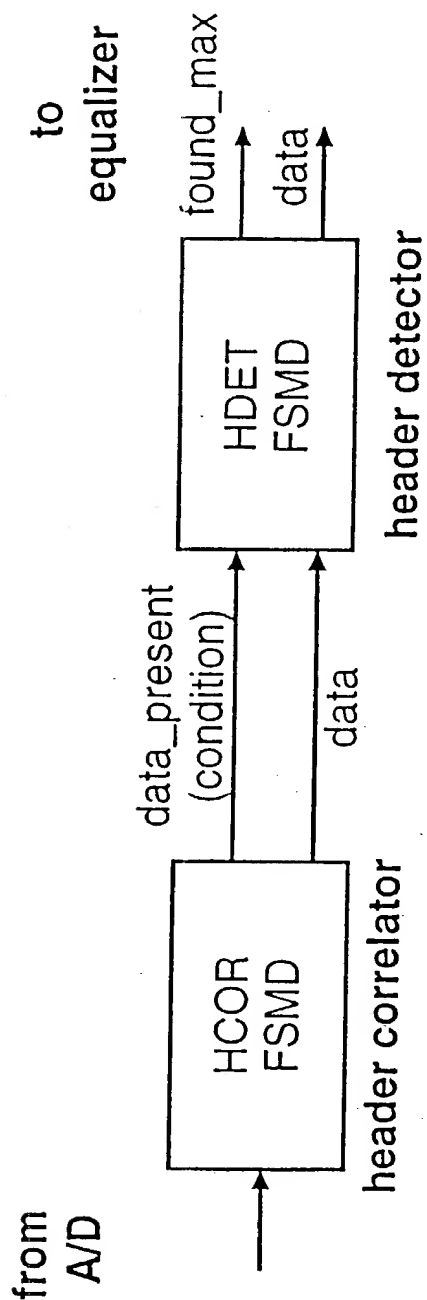


FIG. 20



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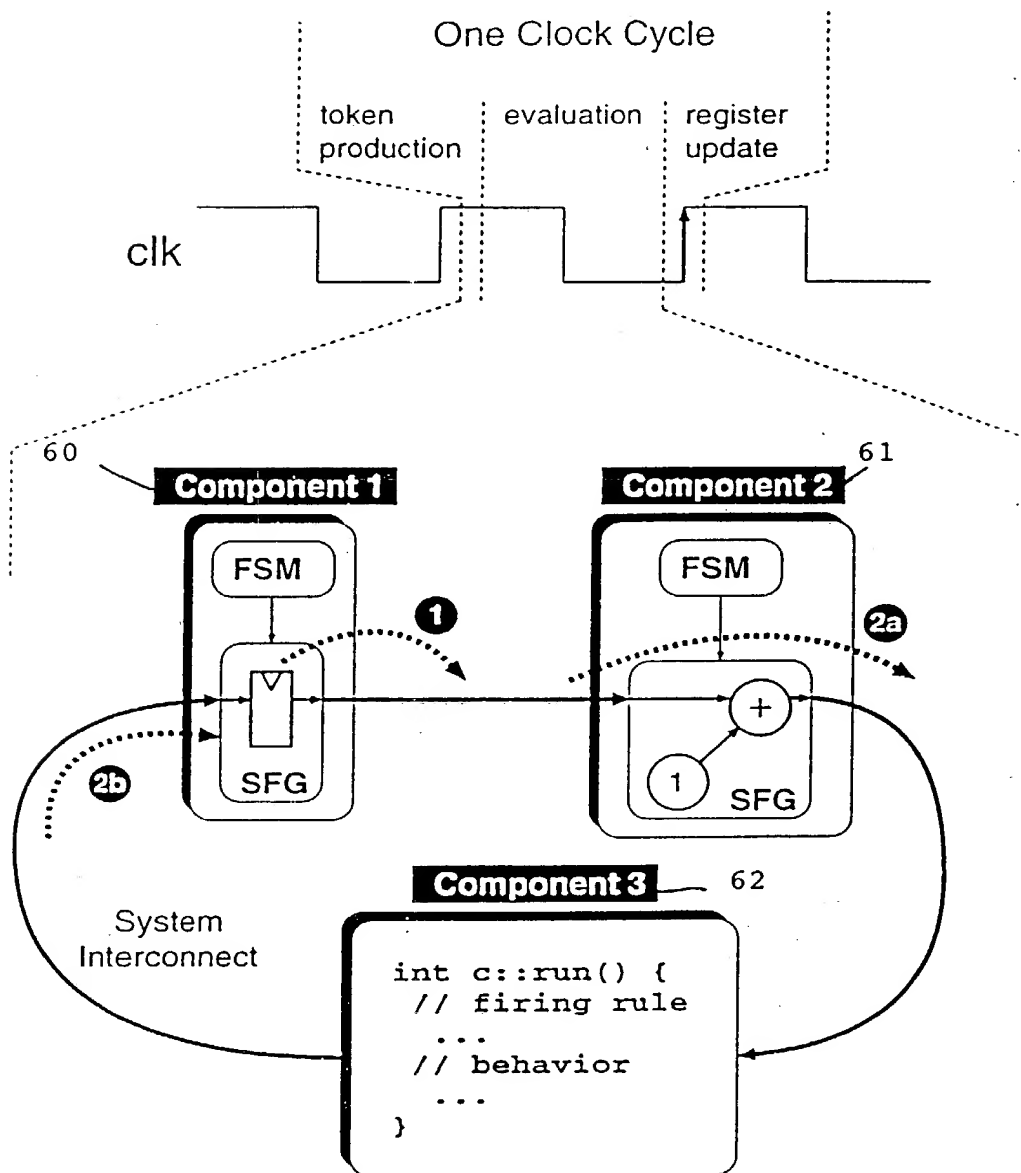


FIG. 21



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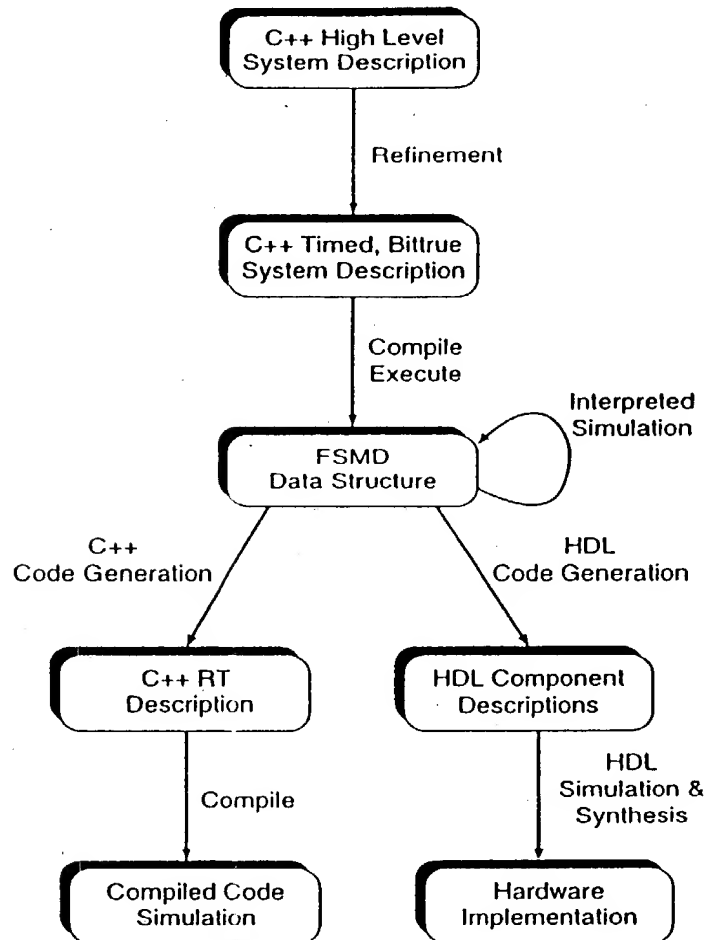


FIG. 22



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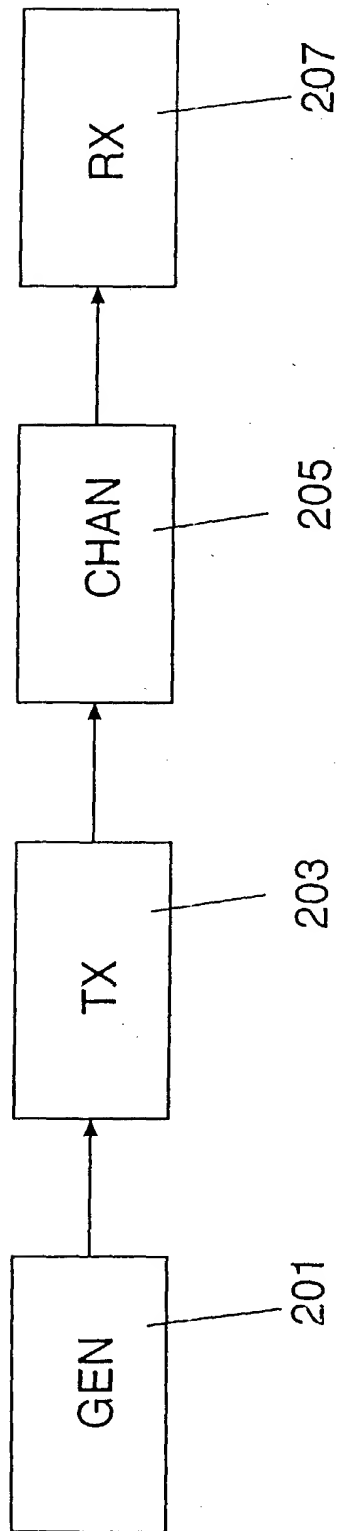


Figure 23.



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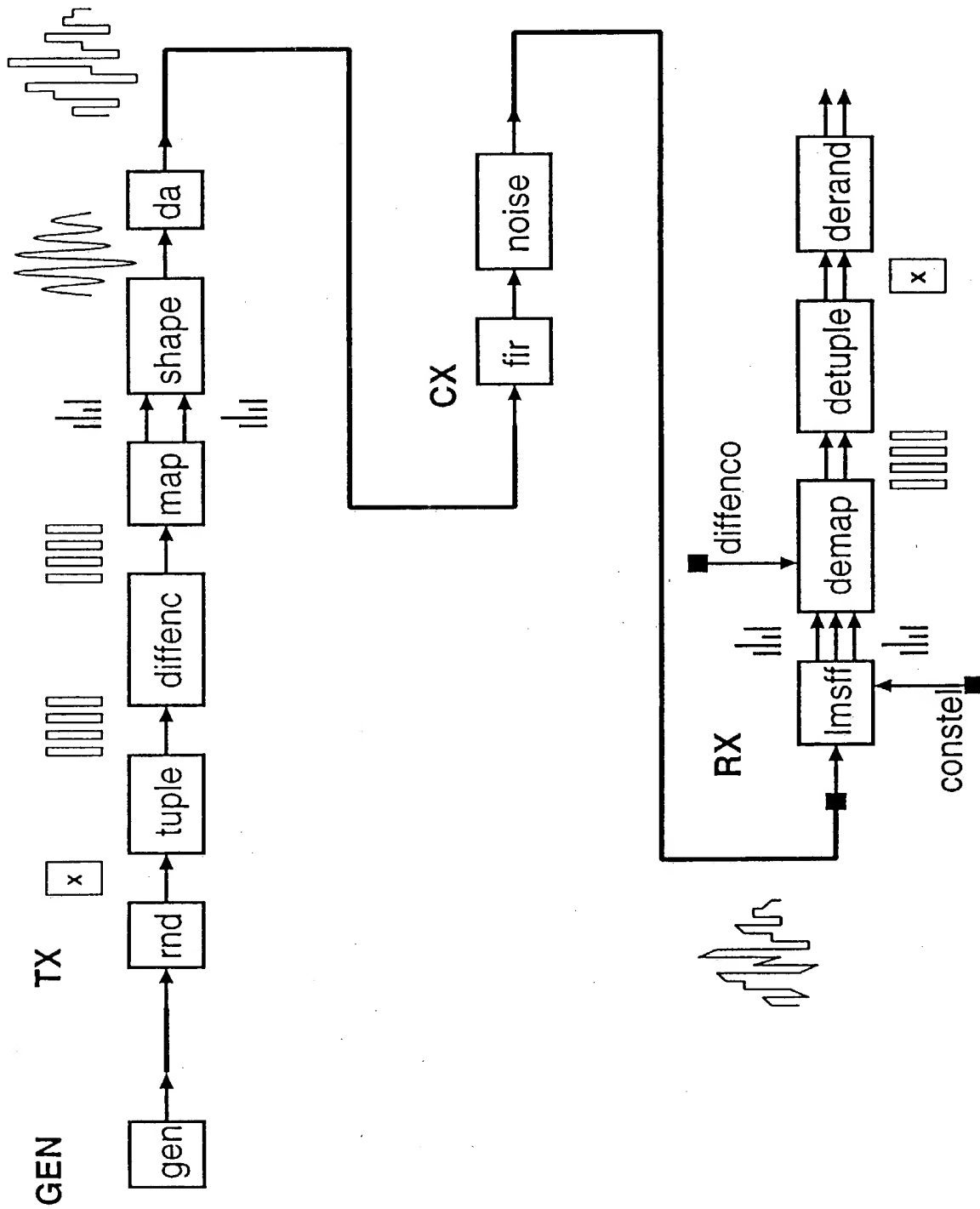


Figure 24.